

**IN THE CLAIMS:**

Claims 2 and 5 have been AMENDED to read as follows:

2. (AMENDED) The semiconductor memory according to claim 1, wherein  
a negative voltage is applied to said first source/drain region [having a diode structure in]  
for erasing.

5. (AMENDED) The semiconductor memory according to claim [1] 3, wherein  
said second impurity region is capacitively coupled with said floating gate electrode  
through a first insulator film.